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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,059	06/24/2003	Charles N. Perez	BUR920030032US1	1058

28211 7590 04/12/2006

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,059	PEREZ ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,13,15-17,25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,13,15-17,25,and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication Applicant's Amendment filed 02/02/2006, claims 1, 3-5, 13, 15-17, 25, and 27-29 are pending.

Claims 1, 13, and 25 have been amended.

Claim Objections

2. Claim 3-4, 13, 15-16, and 27-28 are objected to because of the following informalities:

As per claims 3-4, 15-16, and 27-28 are duplicated to the further limitation of their independent claims.

As per claim 13, line 9, changes "a cell having a guard ring" to "a cell having said guard ring".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1,3-5, 13, 15-17, 25, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Becker (US 6,550,047).**

5. **With respect to claims 1 and 25**, Becker discloses a computer storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within an integrated circuit design having logic devices *(computer implemented method) (col. 2, ll. 49-51, col. 3. ll. 13-15, col. 11, ll. 33-35)*, said method comprising:

determining positions of said logic devices within said integrated circuit design *(defining around a core region of the semiconductor chip) (col. 2, ll. 49-55)*;

incorporating said guard ring into said integrated circuit design *(generating I/O cell including N-type and P-type transistors cell slide, which are isolated by a ring region including ring slides and guard ring slides) (col. 7, ll. 1543)*; and

displaying said logic devices and guard ring graphically, semantically, or symbolically in a single display *(a selection table that includes a plurality of variables that are configured to the determine the size of the I/O cell for particular design. The selection table cane be a text or graphical display have any layout, which prompts the user to provide information regarding each of the desired characteristic)(col. 4, ll. 40-67),*

wherein said displaying *(display having any layout/design user interface display) (col. 4, ll. 50-56 and ll. 64-6)* of said logic device *(N-type transistor slices [202], and P-type transistor slices [204]) (figures 3 and 4)* and said guard ring symbolically *(N-tap and P-tap guard rings [306], corner guard ring [304], guard ring strips [308])(figures 3 and 4),* comprises displaying a parameterized symbol *(figures 1A, 3, and 4, col. 7, ll. 15-67 and col. 8, ll. 1-7)* comprising displaying parameters *(tolerance parameter is includes in the*

selection table, which includes the width parameter/ driver strength parameter/ height parameter)(the Abstract), including at least one of a type of circuit *(N-type transistor slices, P-type transistor slices) (figures 3-4, col. 7, ll. 15-67, and col. 8, ll. 1-7)*, a type of said guard ring *(N-tap guard ring, P-tap guard ring, N-tap guard ring strips, P-tap guard ring strips, and corner guard ring) (figures 3, 4 and 6, col. 7, ll. 15-67, col. 8, ll. 1-7, and col. 9, ll. 20-47)*, and an efficiency of said guard ring *(tolerance parameter, the high and width of each cell slices) (the Abstract, figures 5-6, col.8, ll. 8-67, and col. 9, ll. 1-48)*.

6. **With respect to claim 13**, Becker discloses a method of displaying at least one guard ring within a hierarchical *(inherent from the set metal level) (col. 5, ll. 47-53)* an integrated circuit design having logic devices *(computer implemented method) (col. 2, ll. 49-51, col. 3. ll. 13-15, col. 11, ll. 33-35)*, said method comprising:

Establishing positions of said logic devices within a portion *(figure 4)* of hierarchical *(inherent from the set metal level) (col. 5, ll. 47-53)* integrated circuit design *(defining around a core region of the semiconductor chip) (col. 2, ll. 49-55)*;

incorporating said guard ring into said portion *(figure 4)* integrated circuit design *(generating I/O cell including N-type and P-type transistors cell slide, which are isolated by a ring region including ring slides and guard ring slides) (col. 7, ll. 1543)*; and

displaying said logic devices and guard ring *(display having any layout/design user interface display) (col. 4, ll. 50-56 and ll. 64-6)* graphically, semantically, or symbolically in a single display *(a selection table that includes a plurality of variables that are configured to the determine the size of the I/O cell for particular design. The selection table cane be a text or graphical display have any layout, which prompts the*

user to provide information regarding each of the desired characteristic)(col. 4, ll. 40-67),

displaying *(display having any layout/design user interface display) (col. 4, ll. 50-56 and ll. 64-6)* said portion of said integrated circuit design *(figure 4)* as a cell having said guard ring within a hierarchical *(inherent from the set metal level) (col. 5, ll. 47-53)* integrated circuit design, wherein said displaying of said portion of said integrated circuit design comprises symbolically displaying a parameterized symbol comprising displaying parameters, including at least one of a type of circuit *(N-type transistor slices [202], and P-type transistor slices [204]) (figures 3 and 4)*, a type of said guard ring *(N-tap guard ring, P-tap guard ring, N-tap guard ring strips, P-tap guard ring strips, and corner guard ring) (figures 3, 4 and 6, col. 7, ll. 15-67, col. 8, ll. 1-7, and col. 9, ll. 20-47)*, and an efficiency of said guard ring *(tolerance parameter, the high and width of each cell slices) (the Abstract, figures 5-6, col.8, ll. 8-67, and col. 9, ll. 1-48)*.

7. **With respect to claims 3, 15, and 27**, Becker discloses all the limitations in set forth claims, wherein said displaying of said parameterized symbol displays parameters including the type of circuit *(N-type transistor slices, P-type transistor slices) (figures 3-4, col. 7, ll. 15-67, and col. 8, ll. 1-7)* and type of guard ring *(N-tap guard ring, P-tap guard ring, N-tap guard ring strips, P-tap guard ring strips, and corner guard ring) (figures 3, 4 and 6, col. 7, ll. 15-67, col. 8, ll. 1-7, and col. 9, ll. 20-47)*.

8. **With respect to claims 4, 16, and 28**, Becker discloses all the limitations in set forth claims, wherein said displaying of said parameterized symbol displays parameters

including the efficiency of said guard ring *(tolerance parameter, the high and width of each cell slices) (the Abstract, figures 5-6, col.8, ll. 8-67, and col. 9, ll. 1-48).*

9. **With respect to claims 5, 17, and 29**, Becker discloses all the limitations in set forth claims wherein said displaying of said logic devices displays and said guard ring graphically comprise illustrating relative position of said logic device and guard ring *(figures 2A-2F, 3, and 4, see their description).*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NMD

JACK CHIANG
SUPERVISORY PATENT EXAMINER